April 14, 2018, 6 - 9 pm	FINAL EXAM
	PAGE NO.: 1 of 5
DEPARTMENT & COURSE NO.: PHYS 2610	TIME: 3 hours
EXAMINATION: Circuit Theory and Introductory Electronics	EXAMINER: W Ens

All questions have equal value, except number 5, which has double weight.

corrected version 1. For the following circuit find the total current supplied by the battery, and the current through R_4 , if V = 10 V, $R_1 = 2 \Omega$, $R_2 = 5 \Omega$, $R_3 = 2 \Omega$, $R_4 = 5 \Omega$, and $R_5 = 10 \Omega$.



2. In the RC circuit shown below, with $R = 15 \text{ k}\Omega$ and $C = 1 \mu\text{F}$, determine the charge on the capacitor 15 ms after the input switches from -5 V to +5 V. What is the limiting output voltage after a long time, and how long will it take to reach 99% of that value? (Assume the input was at -5 V for a long time before it switched.)



3. For the following circuit, give an expression for the output if the input is given by $v_{in} = V_{in} \cos(\omega t)$. What is the ratio of the output amplitude to the input amplitude at zero frequency (dc), at high frequency, and at resonance frequency?



April 14, 2018, 6 - 9 pm	FINAL EXAM
	PAGE NO.: 2 of 5
DEPARTMENT & COURSE NO.: PHYS 2610	TIME: 3 hours
EXAMINATION: Circuit Theory and Introductory Electronics	EXAMINER: W Ens
4 (a) Sketch the output waveform for the following circuit if the inp	ut is sinusoidal Assume the

4. (a) Sketch the output waveform for the following circuit if the input is sinusoidal. Assume the turn-on voltage for the diode is zero.



(b) What is the output of the following circuit if the input is sinusoidal with a peak voltage of 2.0 V? Assume the RC time constant is much longer than the period of the input, and both diodes turn on at zero volts.



Double value 5. (a) For common emitter amplifier shown below, with $V_{CC} = 20 \text{ V}$, $R_1 = 35 \text{ k}\Omega$, $R_2 = 2.8 \text{ k}\Omega$, $R_C = 2.25 \text{ k}\Omega$, $R_E = 250 \Omega$, and $\beta = 100$, what are V_{CE} and I_C at the operating point?



(b) Using the circuit shown for the transistor with $r_{be} = 2000 \Omega$, draw an ac-equivalent circuit for the amplifier, and calculate the midband gain, the input impedance, and the output impedance.



- (c) What value for C_1 would result in 3 dB decrease in the gain at 20 Hz from its value at midband, not considering attenuation from other parts of the circuit.
- (d) If C_E were removed, and the output taken from the emitter, what would the voltage gain be?

April 14, 2018, 6 - 9 pm	FINAL EXAM
	PAGE NO.: 3 of 5
DEPARTMENT & COURSE NO.: PHYS 2610	TIME: 3 hours
EXAMINATION: Circuit Theory and Introductory Electronics	EXAMINER: W Ens

6. Show that the output of the circuit below is approximately proportional to the integral of the input, and give the condition for the validity of the approximation.



Draw the circuit for a passive integrator, and give the condition for its validity.

7. (a) Draw the schematic diagram for an inverting amplifier with a gain of -75 and in input impedance of 5 k Ω , using an op-amp.

(b) Draw a circuit diagram for a simple inverter (NOT gate) using one npn transistor and resistors. Practical gates add additional stages for more speed and to reduce the output impedance. Explain what limits the switching speed and output impedance of your single transistor gate.

8. (a) For the clocked RS flip-flop shown, with Q = 0, $\overline{Q} = 1$, sketch Q for the CK, R, and S inputs shown. If R is held at 0, sketch Q for the CK and S inputs shown



(b) Use a truth table to prove $\overline{A + B} = \overline{A} \cdot \overline{B}$

9. (a) A half-adder takes two inputs (A, B) and provides two outputs $(A \oplus B, A \cdot B)$. Show how to implement a half adder using only NAND gates.

(b) A full adder takes three inputs (A, B, C) and provides two outputs $(A \oplus B \oplus C, A \cdot B + A \oplus B \cdot C)$. Show how to implement a full adder using two half-adders and NAND gates. Can you make a full adder with 9 NAND gates?

The End

April 14, 2018, 6 - 9 pm	FINAL EXAM
	PAGE NO.: 4 of 5
DEPARTMENT & COURSE NO.: PHYS 2610	TIME: 3 hours
EXAMINATION: Circuit Theory and Introductory Electronics	EXAMINER: W Ens

PHYS 2610: Final Exam Formula Sheet 2017

Current: $i = \frac{dq}{dt} = \int \mathbf{J} \cdot \vec{da}$ Steady state: $\frac{di}{dt} = 0$; $\oint \mathbf{J} \cdot \overrightarrow{da}$ Ohm's law: $\mathbf{J} = \sigma \mathbf{E} = \frac{\mathbf{E}}{\rho} \Rightarrow v = iR$ with $R = \rho \ell / A$ Current density: $\mathbf{J} = ne\vec{v}_d$ Gauss's law: $\oint \mathbf{E} \cdot \overrightarrow{da} = q_{net} / \varepsilon_0$ Electric potential and potential energy: V = U/q; dU = qdVPotential difference and emf: $\int_{a}^{b} \mathbf{E} \cdot \vec{dl} = -(V_{b} - V_{a}); \ \oint \mathbf{E} \cdot \vec{dl} = 0$ Power: P = viCapacitor: q = CV, $U = q^2/(2C)$ Solution to $\frac{dy}{dx} + ax = b$ has the form $y = Ae^{-ax} + b/a$ Faraday's law: $\mathcal{E}_{ind} = \int_{a}^{b} \mathbf{E} \cdot \vec{dl} = -\frac{d}{dt} \int \mathbf{B} \cdot \vec{da} = -L \frac{di}{dt}$ Inductor: $\mathcal{E} = L \frac{di}{dt}$ Magnetic field of ideal solenoid: $B = \mu_0 nI$ Euler's formula: $e^{j\theta} = \cos\theta + j\sin\theta$ Complex impedance: $Z = R + jX = |Z|e^{j\phi}$; $\tilde{v} = Z\tilde{i}$; $v = \text{Re}(\tilde{v}) = Vcos\omega t$ Capacitive impedance: $Z_C = -jX_C = \frac{1}{i\omega C}$ Inductive impedance: $Z_L = jX_L = j\omega L$ Parallel impedance: $\frac{1}{z} = \sum \frac{1}{z_i}$ Series impedance: $Z = \sum Z_i$ Voltage gain: $a = \frac{v_{out}}{v_{in}}$ Gain in dB: $G_{dB} = 20\log \left| \frac{v_2}{v_1} \right|$

April 14, 2018, 6 - 9 pm	FINAL EXAM
	PAGE NO.: 5 of 5
DEPARTMENT & COURSE NO.: PHYS 2610	TIME: 3 hours
EXAMINATION: Circuit Theory and Introductory Electronics	EXAMINER: W Ens
Q Factor: $Q = \omega_0 L/R$	
Schockley diode equation: $I = I_s(e^{eV/\eta kT}-1)$; η is the ideality factor ~	2 for Si
Bipolar transistor current gains: $\alpha = \frac{I_C}{I_E}$; $\beta = \frac{I_C}{I_B}$	
DeMorgan's theorems: $\overline{A + B} = \overline{A} \cdot \overline{B}$; $\overline{A \cdot B} = \overline{A} + \overline{B}$; $A \cdot B = \overline{\overline{A} + \overline{A}}$	$\overline{\overline{B}}; A + B = \overline{\overline{A} \cdot \overline{B}}$
Half adder: $S = A \oplus B$; $C = A \cdot B$	
Full adder: $S_n = A_n \oplus B_n \oplus C_{n-1}$; $C_n = A_n \cdot B_n + C_{n-1} \cdot (A_n \oplus B_n)$	
Ones' complement: complement each bit	
Two's complement: one's complement plus 1	

Phys 2610 (2018) Find Exam Solutions

D equivalent circuit: R,= 252 V=10V $\begin{array}{c}
 I \\
 V \\
 \hline
 I \\
 \hline
 R_1 \\
 \hline
 R_2 \\
 \hline
 R_4 \\
 \hline
 R_5 \\
 V'' \\
 R_5 \\
 V'' \\
 \overline{R_5} \\
 V'' \\
 \overline{R_5} \\$ R2= 552 R3= 252 Ry= 552 R5= 10_2 Equivalent resistance: R = R, + R2//(R3 + R4//R5) Ry//R5 = (5)(10)/(5+10) 2 = 3.33 52 R3 + R4//R5= 2 x + 3.33 x = 5.33 x R211 (R3+R4/1R5) = (5) (5.33)/(5+5.33) SI = 2.58 SI R= 2 r + 2.58 r = 4.58 r Current supplied by battery: I = K = 10V 4.5852 = 2.18A Then V'= V-IR1 = 10V- (2.18A) (22) = 5.64V and $V'' = \frac{V'(R_4/R_5)}{R_3 + R_4/R_5} = \frac{5.64V(3.33 r)}{5.33 r} = 3.52V$ Do IH= V"/RH= 3.52V/55 = 0.705A

$$V_{0} = 5V$$

$$(2)$$

$$V_{0} = 5V$$

$$(2)$$

$$V_{0} = \frac{1}{2}V_{0} = \frac{1}{R}C = \frac{1}{2}V_{0} = \frac{1}{R}C =$$

3 R L Nout Voltage dividen: Nout = Nin Z where $Z = \bot + jwL$ R+Z= j (WL-1/wc) The ratio of amplitudes is then $\frac{V_{out}}{V_{in}} = \frac{|\nu v_{out}|}{|\nu v_{in}|} = \frac{|z|}{|R+z|} = \frac{(\omega L - 1/\omega c)}{\sqrt{R^2 + (\omega L - 1/\omega c)^2}}$ For w=0, Vout -> 1/wc -> 1 Vin 1/wc (C presente s impedance) (L presente so impedance) Forward, Vout -> WL -> 1 For w = 1/Jic, Vout = 0 (LC is short cet)

(a) m t Nout Nin= Vo cowt When B first goes positive w.r.t. A the diode closer and the capacitor charger to the peak voltage. +V, (When B decreaser, the diode open and the capacitor has no path to discharge, so it maintains the voltage Vo, acting like a battery. Subrequently, the diode only open when vin reacher - Vo (or slightly before if the capacitor leaks a small amount of charge). Nin a Nont => Nont = Nin + Vo 2Vot Nontz 2Vot Nont Vo Nont -Vot Nin -Vot The second diode is a closed switch until Cz changer to the maximum output of the first stege, which is 2Vo from part (a) (assuming C, doer not discharge apprecially through R). C2 has no path to discharge and so holds the voltage 2 Vo = 4V.

(c) C, forme a high pass filter with rin. For 3 dB attenuation at 20 Hz due to this filter: $W_{3dB} = \pi C_1 = 2\pi f_{3dB} \pi m = 7.2\mu F$ (d) The gain for an emitter follower is unity, since VE=VB-VBE and VBE is ~ constant -> Ne = Nb o Nout = Nin

C R 7911 Nin + Sout Since N = N+, N== 0 (virtual ground) Then Nont = -g/c = - the Sidt But vin = iR so Nout = -1 SNindt This is valid for 1 a. | >> (a) or a, >> 1/wc on wRC >> 1/2. A parime integrator is a R Vin C Vont Here Nont = g/c = t Sidt and Nin-iR=Nout => i= R (Nin - Nout). The for Nort << Nin, i= Rc S Nim dt The condition Nont << Nin => /we << R => wrc >> 1

a Ri Tomo (J) (a) $Rin = \frac{Vin}{L} = R_1$ pince $N_2 = N_4 = 0$ Input impedance: -> R.= 5.kr $Gain: a = -\frac{R_2}{R_1} \rightarrow R_2 = -aR_1 = -(-75)(5k_2) = 375k_2$ (b) muta: Rz is needed to limit the current when the transistor is on, but it limits the speed because the effective rapacitance of the transistor must charge through Rz when it turn off. Rz is also the output impedance which limits the load that it can drive.



