UNIVERSITY OF MANITOBA

April 11, 2019, 9 am - 12 noon | FINAL EXAM

DEPARTMENT & COURSE NO.: PHYS 2610 | TIME: 3 hours

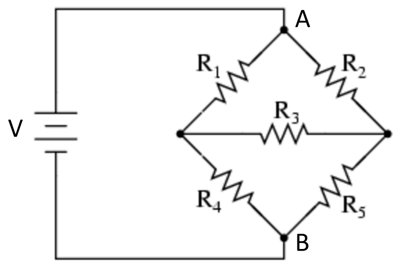
EXAMINATION: Circuit Theory and Introductory Electronics | EXAMINER: W Ens

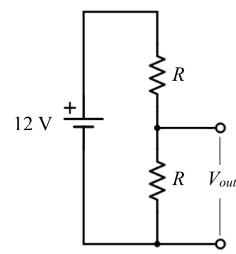
One letter-sized sheet of notes (both sides) is permitted.
Questions 4 and 7 are worth 15 marks. All the others are worth 10. The total is 100.

10 marks 1. (a) In the circuit shown below left, what is the current in R_3 if $\frac{R_1}{R_4} = \frac{R_2}{R_5}$?

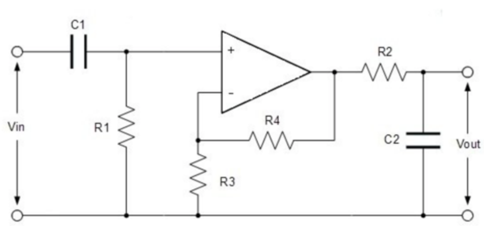
(b) In the same circuit, what is the equivalent resistance between points A and B if $\frac{R_1}{R_4} = \frac{R_2}{R_5}$?

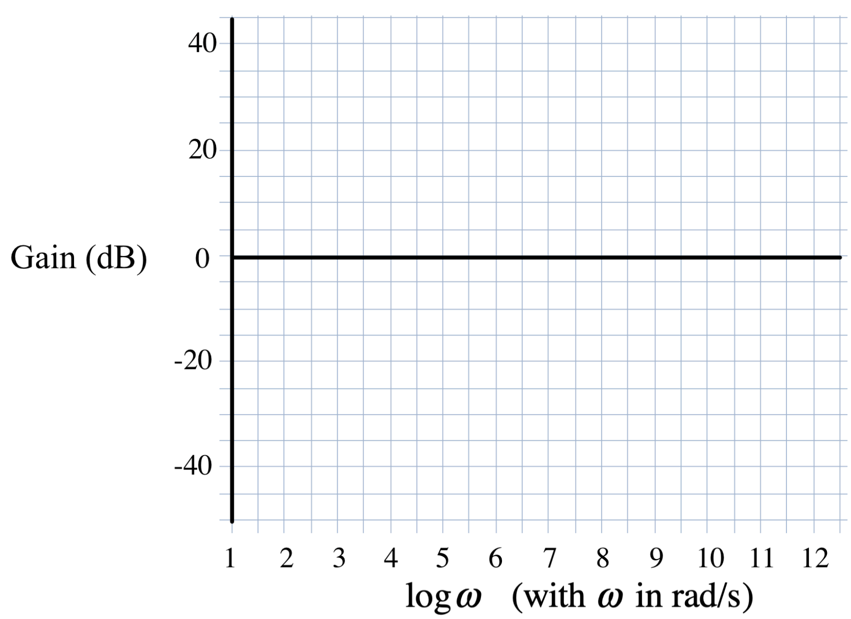
(c) For the circuit shown below right, what would a voltmeter with a 1 MΩ input resistance read across V_{out} if (i) R = 1 kΩ, and if (ii) R = 1 MΩ



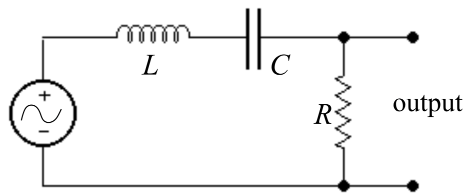


10 marks 2. For the band pass filter shown below, sketch the gain in dB as a function of the log of the angular frequency ω (in rad/s). Make the sketch to scale on the graph provided. Use C_1 = 1 μF, R_1 = 1 kΩ, C_2 = 100 pF and R_2 = 10 kΩ. Take R_4 = 0, so the op amp simply acts as a voltage follower allowing the two RC filters to be treated independently.

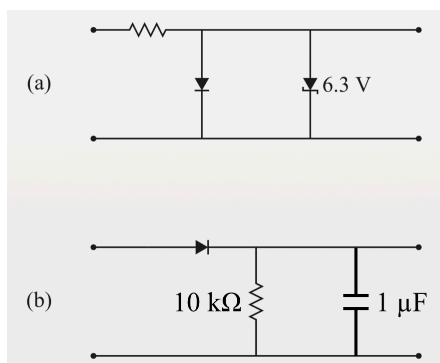




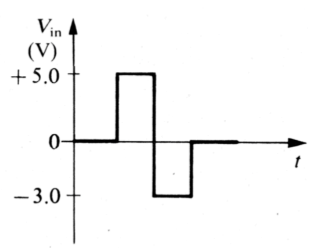
10 marks 3. For the RLC circuit shown, find the Thevenin equivalent circuit if $L = 100$ mH, $R = 400\ \Omega$, $C = 1\ \mu$F, and the input is sinusoidal with an angular frequency of 2000 rad/s and an amplitude of 10 V. What load impedance will ensure maximum power transfer? What is the equivalent circuit at resonance?

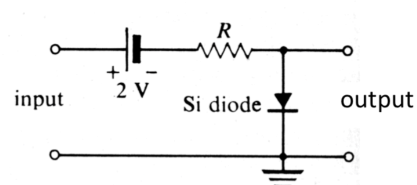


15 marks 4. Sketch the output waveforms expected when a 100 Hz, 10 V (peak) sine wave is applied to the circuits (a) and (b) below. Specify important voltage levels and time scales. The input is on the left and the output is on the right.



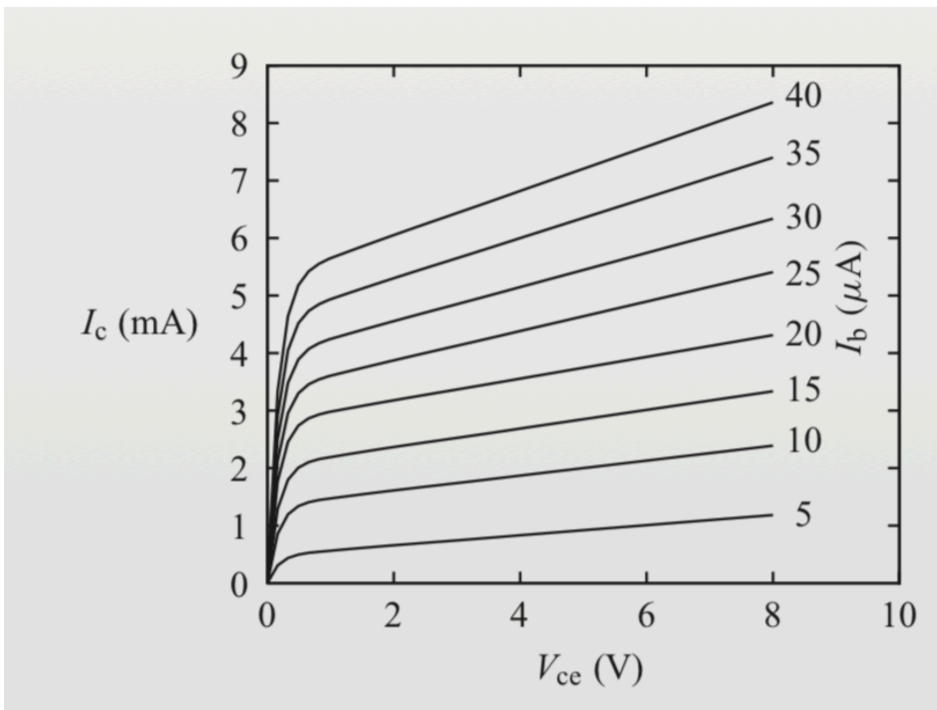
(c) Sketch the output waveform to scale for the following circuit with the input as shown.





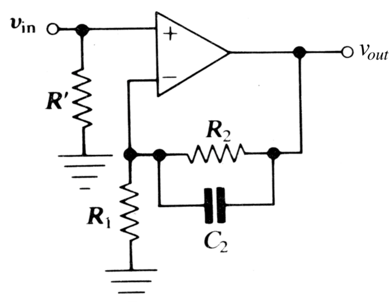
10 marks 5. (a) Design an H-biased common emitter amplifier circuit with a gain of 5, that will set a reasonable operating point for a transistor with the characteristics shown below. What is the approximate maximum input signal amplitude that can be used before the output is clipped or distorted?

(b) How would you change the biasing to use the same transistor in an emitter follower amplifier?

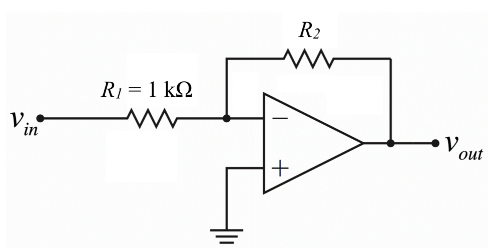


10 marks 6. Draw a simplified ac equivalent circuit for the amplifier of question 5a, and estimate the midband voltage gain and input and output impedances. Use $r_{be} = 1\ \text{k}\Omega$. How would the gain and input impedance change if a bypass capacitor were used across the emitter resistor?

15 marks 7. (a) Find the complex gain for the following circuit when $\omega = 1/R_2C_2$.



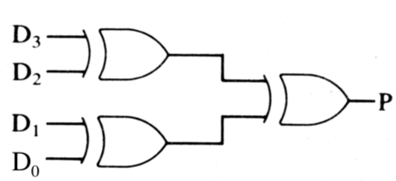
(b) When the open loop gain of an op amp is considered to be finite, the gain of the inverting amplifier below is given by $a = \frac{-a_o R_2}{R_1 + R_2 + a_o R_1}$. Suppose the magnitude of the gain decreases by 3 dB from its dc value at a frequency of 100 kHz when R_2 = 1.0 kΩ. What will be the 3-dB frequency for R_2 = 100 kΩ? Assume the open loop gain decreases at 20 dB per decade.



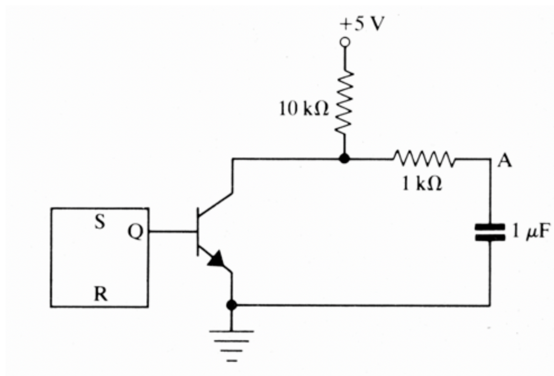
(c) Design an op-amp circuit that will take the derivative of one signal and add it to the integral of a second signal. It is not necessary to specify component values.

10 marks 8. (a) A half adder takes two inputs (A, B) and generates two outputs ($A \cdot B$, $A \oplus B$). Using $A \oplus B = \overline{\overline{A + B} + A \cdot B}$, show how to implement a half adder using 3 gates selected from AND, NAND, OR, and NOR. A full adder takes three inputs (A, B, C) and provides two outputs ($A \oplus B \oplus C, A \cdot B + A \oplus B \cdot C$). Show how to implement a full adder using 7 gates.

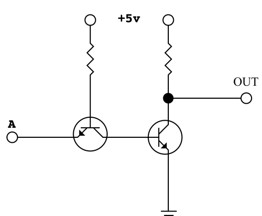
(b) Write the truth table for the following gate schematic. (P is called the parity.)



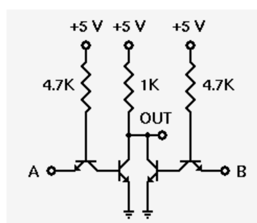
10 marks 9. (a) Initially $R = S = Q = 0$V on the RS flip flop shown below. At time $t = 0$, S goes to 1. Sketch v_A as a function of time.



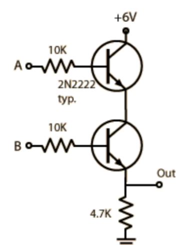
(b) Identify the function of each of the following gates.



(a)



(b)



(c)

The End

PHYS 2610: Final Exam Formula Sheet 2017

Current: $i = \frac{dq}{dt} = \int \mathbf{J} \cdot \overrightarrow{da}$

Steady state: $\frac{di}{dt} = 0; \oint \mathbf{J} \cdot \overrightarrow{da}$

Ohm's law: $\mathbf{J} = \sigma\mathbf{E} = \frac{\mathbf{E}}{\rho} \Rightarrow v = iR$ with $R = \rho\ell/A$

Current density: $\mathbf{J} = ne\vec{v}_d$

Gauss's law: $\oint \mathbf{E} \cdot \overrightarrow{da} = q_{net}/\varepsilon_0$

Electric potential and potential energy: $V = U/q;\ dU = qdV$

Potential difference and emf: $\int_a^b \mathbf{E} \cdot \overrightarrow{dl} = -(V_b - V_a);\ \oint \mathbf{E} \cdot \overrightarrow{dl} = 0$

Power: $P = vi$

Capacitor: $q = CV,\ U = q^2/(2C)$

Solution to $\frac{dy}{dx} + ax = b$ has the form $y = Ae^{-ax} + b/a$

Faraday's law: $\mathcal{E}_{ind} = \int_a^b \mathbf{E} \cdot \overrightarrow{dl} = -\frac{d}{dt}\int \mathbf{B} \cdot \overrightarrow{da} = -L\frac{di}{dt}$

Inductor: $\mathcal{E} = L\frac{di}{dt}$

Magnetic field of ideal solenoid: $B = \mu_0 nI$

Euler's formula: $e^{j\theta} = \cos\theta + j\sin\theta$

Complex impedance: $Z = R + jX = |Z|e^{j\phi};\ \tilde{v} = Z\tilde{\imath};\ v = \mathrm{Re}(\tilde{v}) = Vcos\omega t$

Capacitive impedance: $Z_C = -jX_C = \frac{1}{j\omega C}$

Inductive impedance: $Z_L = jX_L = j\omega L$

Series impedance: $Z = \sum Z_i$

Parallel impedance: $\frac{1}{Z} = \sum \frac{1}{Z_i}$

Voltage gain: $a = \frac{v_{out}}{v_{in}}$

Gain in dB: $G_{dB} = 20\log\left|\frac{v_2}{v_1}\right|$

Q Factor: $Q = \omega_0 L/R$

Schockley diode equation: $I = I_s(e^{eV/\eta kT}$-1); η is the ideality factor ~ 2 for Si

Bipolar transistor current gains: $\alpha = \frac{I_C}{I_E}$; $\beta = \frac{I_C}{I_B}$

DeMorgan's theorems: $\overline{A+B} = \bar{A} \cdot \bar{B}$; $\overline{A \cdot B} = \bar{A} + \bar{B}$; $A \cdot B = \overline{\bar{A} + \bar{B}}$; $A + B = \overline{\bar{A} \cdot \bar{B}}$

Half adder: $S = A \oplus B$; $C = A \cdot B$

Full adder: $S_n = A_n \oplus B_n \oplus C_{n-1}$; $C_n = A_n \cdot B_n + C_{n-1} \cdot (A_n \oplus B_n)$

Ones' complement: complement each bit

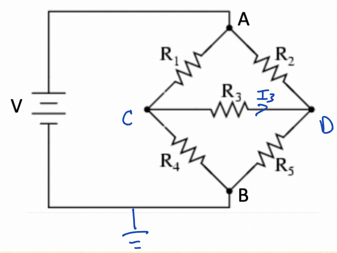
Two's complement: one's complement plus 1

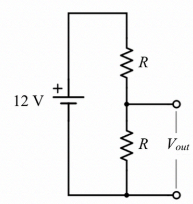
Phys2610 (2019) Final Exam solutions

1. (a) In the circuit shown below left, what is the current in R_3 if $\frac{R_1}{R_4} = \frac{R_2}{R_5}$?

   (b) In the same circuit, what is the equivalent resistance between points A and B if $\frac{R_1}{R_4} = \frac{R_2}{R_5}$?

   (c) For the circuit shown below right, what would a voltmeter with a 1 MΩ input resistance read across V_{out} if (i) R = 1 kΩ, and if (ii) R = 1 MΩ





(a) With R_3 removed, $V_C = V \frac{R_4}{R_1+R_4} = V \frac{1}{1+R_4/R_1}$ & $V_D = V \frac{1}{1+R_5/R_2}$

$\Rightarrow V_C = V_D$ if $\frac{R_4}{R_1} = \frac{R_5}{R_2}$. $\quad \therefore \boxed{I_3 = 0}$

(Note the Thevenin voltage between C & D with R_3 removed is $V_{th} = V_C - V_D = 0$)

(b) If $I_3 = 0$, R_3 can be ignored $\Rightarrow \boxed{R_{AB} = (R_1+R_4)//(R_2+R_5)}$ [1]

R_3 can also be shorted $\Rightarrow \boxed{R_{AB} = R_1//R_2 + R_4//R_5}$ [2]

Either result, without simplification is good for full credit, but both reduce to the same simpler expression using $\frac{R_1}{R_4} = \frac{R_2}{R_5}$:

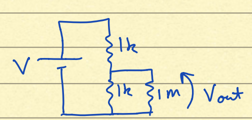
$[1] = (R_1+R_4)//(R_2+R_5) = \left(\frac{1}{R_1+R_4} + \frac{1}{R_2+R_5}\right)^{-1}$ but $\frac{1}{R_2+R_5} = \frac{1}{R_2+R_2R_4/R_1} = \frac{R_1}{R_2(R_1+R_4)}$ using $R_5 = R_2R_4/R_1$

so $R_{AB} = \left(\frac{R_2+R_1}{R_2(R_1+R_4)}\right)^{-1} = \frac{R_2(R_1+R_4)}{R_1+R_2}$

$[2] = R_1//R_2 + R_4//R_5 = \frac{R_1R_2}{R_1+R_2} + \frac{R_4R_5}{R_4+R_5}$ but $\frac{R_4R_5}{R_4+R_5} = \frac{R_4R_2R_4/R_1}{R_4+R_2R_4/R_1} = \frac{R_2R_4}{R_1+R_2}$ using $R_5 = R_2R_4/R_1$

so $R_{AB} = \frac{R_2(R_1+R_4)}{R_1+R_2}$

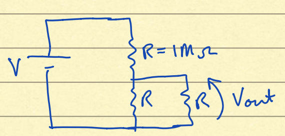
(c) (i)



$V_{out} = \frac{1}{2}(12V) = \boxed{6V}$

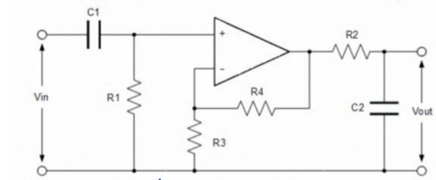
or $V_{out} = V \frac{1M//1k}{1k + 1M//1k} = V \frac{999}{1999} = 5.997V$

(ii)



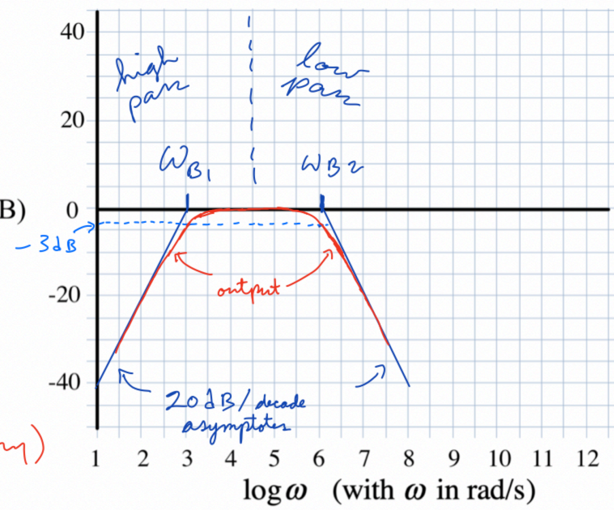
$V_{out} = V_{in} \frac{R//R}{R+R//R} = V_{in} \frac{R/2}{3/2 R} = \frac{V_{in}}{3} = \boxed{4V}$

2. For the band pass filter shown below, sketch the gain in dB as a function of the log of the angular frequency ω (in rad/s). Make the sketch to scale on the graph provided. Use $C_1 = 1\ \mu F$, $R_1 = 1\ k\Omega$, $C_2 = 100$ pF and $R_2 = 10\ k\Omega$. Take $R_4 = 0$, so the op amp simply acts as a voltage follower allowing the two RC filters to be treated independently.



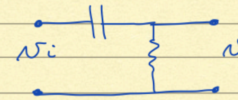
high pass
$R_1C_1 = 10^{-3}s \Rightarrow \omega_{B_1} = 10^3$ rad/s
For $\omega = \omega_{B_1}$, $G_{dB} = -3$ dB
For $\omega >> \omega_{B_1}$, $G_{dB} = 0$
For $\omega << \omega_{B_1}$, -20 dB/decade

low pass
$R_2C_2 = 10^{-6}s \Rightarrow \omega_{B_2} = 10^6$ rad/s
For $\omega = \omega_B$, $G_{dB} = -3$ dB
For $\omega << \omega_B$, $G_{dB} = 0$
For $\omega >> \omega_B$, -20 dB/decade.



(only the graph & ω_B's needed for full credit; material below is expository)

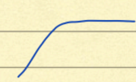
1st filter: high pass



$$v_o = \frac{v_i R}{R + 1/j\omega C} = \frac{v_i R}{|Z| e^{j\theta}}$$

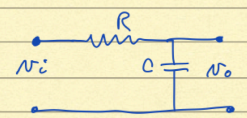
$$\Rightarrow |a| = \frac{R}{\sqrt{R^2 + (1/\omega C)^2}} = \frac{\omega RC}{\sqrt{1 + (\omega RC)^2}}$$

so
$\omega = 1/RC \Rightarrow |a| = 1/\sqrt{2}$
$\omega >> 1/RC \Rightarrow |a| = 1$
$\omega << 1/RC \Rightarrow |a| = \omega RC$
$\Rightarrow 20 \log|a| = 20 \log RC + 20 \log \omega$



Here $\omega_{B_1} = 1/R_1C_1 = 10^3$ rad/s

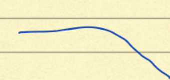
2nd filter: low pass



$$v_o = v_i \frac{(1/j\omega C)}{R + 1/j\omega C} = \frac{v_i}{(1 + j\omega RC)}$$

$$\Rightarrow |a| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

so
$\omega = 1/RC \Rightarrow |a| = 1/\sqrt{2}$
$\omega << 1/RC \Rightarrow |a| = 1$
$\omega >> 1/RC \Rightarrow |a| = 1/\omega RC$
$\Rightarrow 20 \log|a| = -20 \log RC - 20 \log \omega$



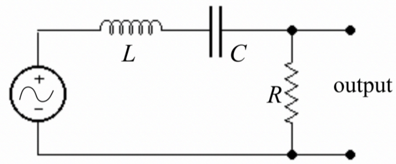
Here $\omega_{B_2} = 1/R_2C_2 = 10^6$ rad/s

Overall gain is product $a = a_1 a_2$ or the sum in dB $G_{dB} = G_{dB1} + G_{dB2}$

But when one gain is not unity ($G_{dB} \neq 0$), the other is unity ($G_{dB} = 0$), so combining is straightforward

3. For the RLC circuit shown, find the Thevenin equivalent circuit if $L = 100$ mH, $R = 400\ \Omega$, $C = 1\ \mu$F, and the input is sinusoidal with an angular frequency of 2000 rad/s and an amplitude of 10 V. What load impedance will ensure maximum power transfer? What is the equivalent circuit at resonance?

$v_i = V_i e^{j\omega t}$



Thevenin voltage $= \text{open cct output} = \dfrac{v_i R}{z}$ where $z = R + j(\omega L - 1/\omega C) = |z|\, e^{j\theta}$

where $|z| = \sqrt{R^2 + (\omega L - 1/\omega C)^2}$ & $\tan\theta = \dfrac{\omega L - 1/\omega C}{R}$

So $\boxed{v_{th} = \dfrac{V_i R}{|z|} e^{j(\omega t - \theta)}}$

Using the given values, $X_L = \omega L = (2000)(100\times 10^{-3})\ \Omega = 200\ \Omega$

$X_C = 1/\omega C = 1/(2000)(10^{-6})\ \Omega = 500\ \Omega$

so $|z| = \sqrt{R^2 + (X_L - X_C)^2} = \sqrt{400^2 + (200-500)^2}\ \Omega = 500\ \Omega$

& $\theta = \arctan \dfrac{X_L - X_C}{R} = \arctan\left(\dfrac{-300}{400}\right) = -37°$ or -0.643 rad

so $\boxed{v_{th} = (8\text{V})\ e^{j(\omega t + 0.643)}}$ (magnitude is enough for full credit)

Thevenin Impedance = resistance with voltage source replaced by a short cct.

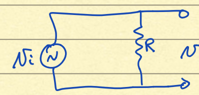
$= \boxed{R // j(\omega L - \omega C)}$

Using the given values, $z_{th} = 400\Omega // j(-300\Omega) = \dfrac{-120000j}{400-300j}\ \Omega = \dfrac{-1.2k\ j\ (4+3j)}{5^2}\ \Omega$

$= \dfrac{3.6k}{25} - \dfrac{4.8k}{25} j\ \Omega = \boxed{144 - 192j\ \Omega}$

Max power transfer: $\boxed{z_L = z_{th}^* = 144 + 192j\ \Omega}$

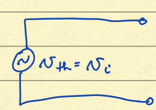
Resonance: $X_L = X_C \Rightarrow$



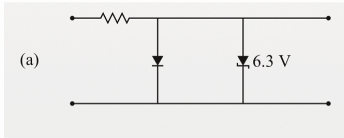
Then $\boxed{v_{th} = v_o = v_i}$

and $\boxed{z_{th} = R // 0 = 0}$

eq't cct:

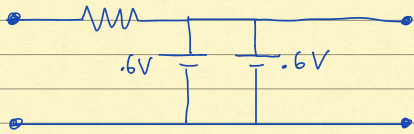


4. Sketch the output waveforms expected when a 100 Hz, 10 V (peak) sine wave is applied to the circuits (a) and (b) below. Specify important voltage levels and time scales. The input is on the left and the output is on the right.



For input > 0.6V, both diodes turn on, so the equiv. circuit is:

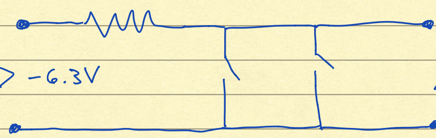
$v_{in} > .6V$



$v_{out} = +.6V$

For 0.6V > input > −6.3V, both diodes are off:

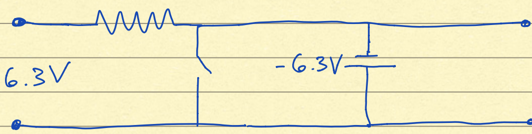
0.6V > v_{in} > −6.3V



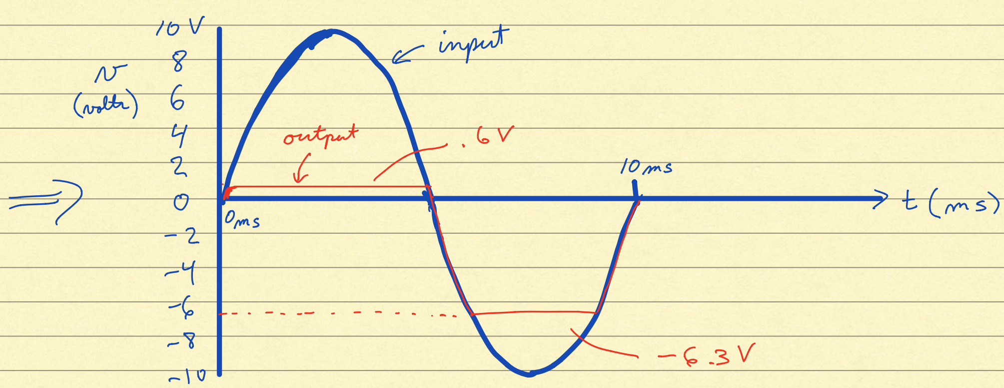
$v_{out} = v_{in}$

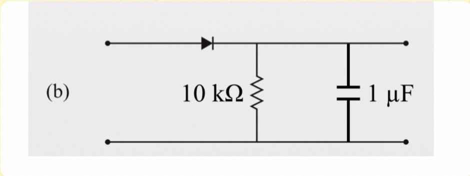
For input < −6.3V, the zener breaks down:

v_{in} < −6.3V



v_{out} = −6.3V

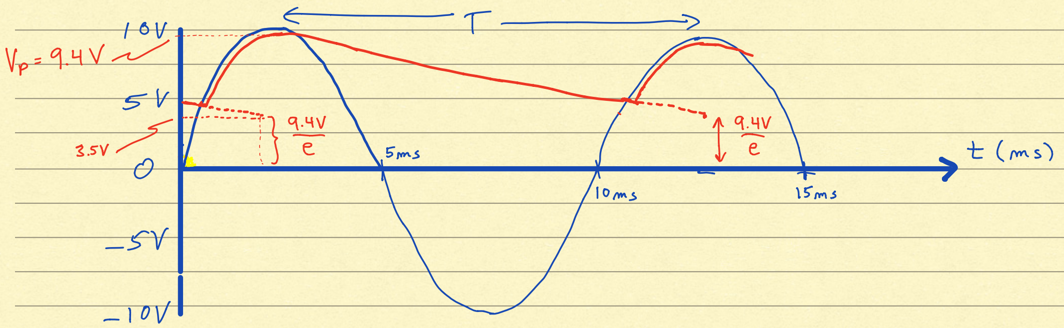




This is a filtered ½ wave rectifier.

Input period: $T = 1/f = 1/100\,Hz = 10\,ms$

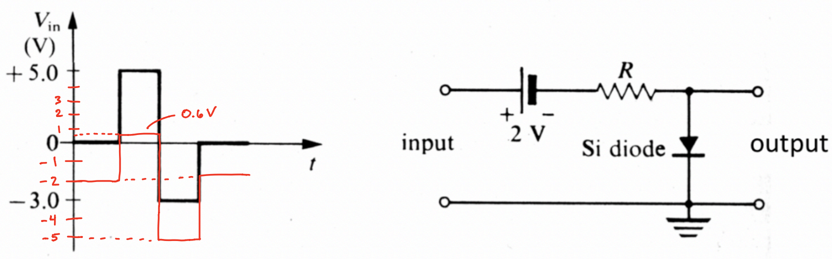
RC time const: $\tau = RC = 10k\Omega \cdot 1\mu F = 10\,ms$



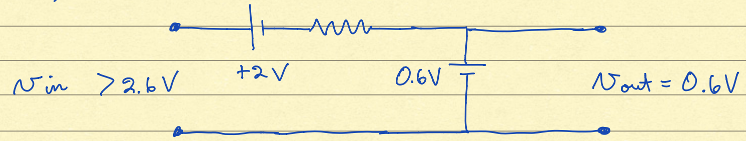
The peak output is $V_p = V_{in} - V_t = 9.4V$

The decay: $v_{out} = V_p e^{-t/\tau} \Rightarrow$ for $t = T = \tau$, $v_{out} = V_p/e = 3.5V$

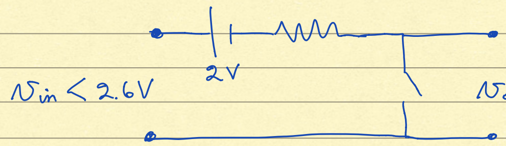
(c) Sketch the output waveform to scale for the following circuit with the input as shown.



For input > 2.6V, the diode turn on:

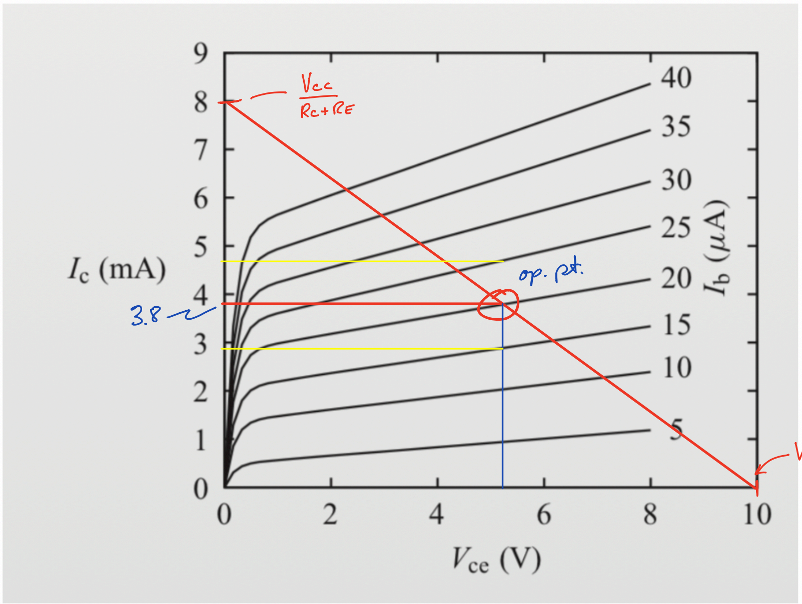


For input < 2.6V, the diode is off:



5. (a) Design an H-biased common emitter amplifier circuit with a gain of 5, that will set a reasonable operating point for a transistor with the characteristics shown below. What is the approximate maximum input signal amplitude that can be used before the output is clipped or distorted?

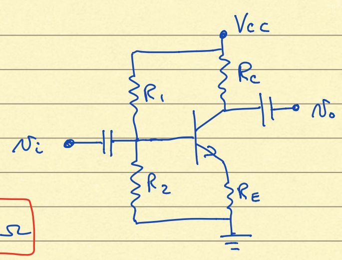
(b) How would you change the biasing to use the same transistor in an emitter follower amplifier?



$\beta_{ac} = \frac{\Delta I_c}{\Delta I_b} \cong \frac{(4.7-2.8)\,mA}{(25-15)\,\mu A}$

$= 190$

(a) From load line + op. point shown,



load line:

$V_{cc} - I_c(R_C+R_E) - V_{CE} = 0$

$\rightarrow I_c = \frac{V_{cc}}{R_C+R_E} - \frac{V_{CE}}{R_C+R_E}$

① $\boxed{V_{cc} = 10V}$ and $R_C + R_E = \frac{V_{cc}}{8mA} = 1.25k\Omega$

② For a gain of (-)5, $R_C/R_E = 5$

Then $5R_E + R_E = 1.25k\Omega \Rightarrow \boxed{R_E = 208\Omega}$

and $R_C = 1.25k\Omega - R_E \Rightarrow \boxed{R_C = 1042\Omega}$

③ At op. pt. $I_C \cong I_E = 3.8mA$ so $V_E = I_E R_E = 0.79V \rightarrow V_B = V_E + 0.6V = 1.39V$

④ $V_B = V_{cc}\frac{R_2}{R_1+R_2}$ if $I_2 >> I_B$. Choosing $I_2 = 20\, I_B$ at the op. pt, $I_2 = 20\,(20\mu A) = 0.4mA$

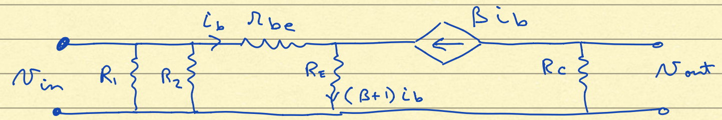
Since $V_B = I_2 R_2$, $R_2 = V_B/I_2 = 1.39V/0.4mA \Rightarrow \boxed{R_2 = 3.48k\Omega}$

Also $I_2 = \frac{V_{cc}-V_B}{R_1} \Rightarrow R_1 = \frac{V_{cc}-V_B}{I_2} = \frac{(10-1.39)V}{0.4mA} \Rightarrow \boxed{R_1 = 21.5k\Omega}$

The output amplitude cannot exceed ~4.5V, so the input must be smaller than $\frac{4.5V}{5} = \boxed{0.9V}$.

(b) For an emitter follower, R_C is removed so $R_E = 1.25k\Omega$ to give the same operating pt. This would raise V_E to $I_C R_E = 4.75V$ + V_B to $5.35V$. Then $R_1 + R_2$ would be changed to provide this voltage.

6. Draw a simplified ac equivalent circuit for the amplifier of question 5a, and estimate the midband voltage gain and input and output impedances. Use $r_{be} = 1\ \text{k}\Omega$. How would the gain and input impedance change if a bypass capacitor were used across the emitter resistor?



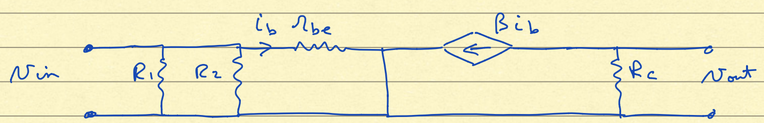
gain: $a = \dfrac{v_{out}}{v_{in}} = \dfrac{-\beta i_b R_C}{i_b r_{be} + (\beta+1)R_E} \cong \dfrac{-R_C}{R_E} \rightarrow \boxed{a = -5}$ (by design)

input impedance: $r_{in} = R_1 // R_2 // (r_{be} + (\beta+1)R_E) \cong R_1 // R_2 // \beta R_E = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{\beta R_E}\right)^{-1}$

$\Rightarrow r_{in} = \left(\frac{1}{3.5k} + \frac{1}{21.5k} + \frac{1}{(190)(208)}\right)^{-1} \Omega \rightarrow \boxed{r_{in} = 2.8k\,\Omega}$

output impedance: $r_{out} = \dfrac{v_{out}\,(\text{open})}{i_{out}\,(\text{short})} = \dfrac{-\beta i_b R_C}{-\beta i_b} = R_C \rightarrow \boxed{r_{out} = 1042\,\Omega}$

with bypass capacitor across R_E:

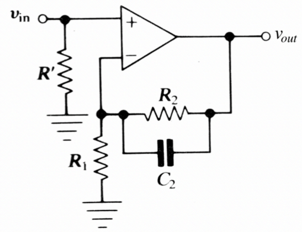


gain: $a = \dfrac{v_{out}}{v_{in}} = \dfrac{-\beta i_b R_C}{i_b r_{be}} = \dfrac{-\beta R_C}{r_{be}} = -\dfrac{(190)(1042)}{1000} \rightarrow \boxed{a = -198}$

input impedance: $r_{in} = R_1 // R_2 // r_{be} = \left(\frac{1}{21.5k} + \frac{1}{3.48k} + \frac{1}{1000}\right)^{-1} \Omega$

$\rightarrow \boxed{r_{in} = 750\,\Omega}$

7. (a) Find the complex gain for the following circuit when $\omega = 1/R_2C_2$.



$v_{in} = v_+ = v_- = \dfrac{v_{out} R_1}{R_1 + z_2}$ where $z_2 = R_2 // (1/j\omega C_2)$

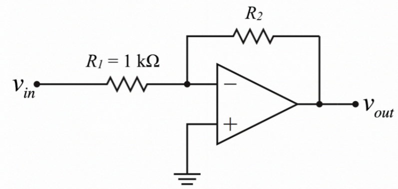
or $z_2 = R_2 // (-jR_2)$ for $\omega = 1/R_2C_2$

$= \dfrac{-jR_2^2}{R_2 - jR_2} = \dfrac{R_2}{1+j}$

$\Rightarrow a = \dfrac{v_{out}}{v_{in}} = \dfrac{R_1 + R_2/(1+j)}{R_1} = \boxed{1 + \dfrac{R_2}{R_1(1+j)}}$

or $a = 1 + \dfrac{R_2(1-j)}{R_1\, 2} = \boxed{\left(1 + \dfrac{R_2}{2R_1}\right) - j\left(\dfrac{R_2}{2R_1}\right)}$

(b) When the open loop gain of an op amp is considered to be finite, the gain of the inverting amplifier below is given by $a = \frac{-a_o R_2}{R_1 + R_2 + a_o R_1}$ ★ Suppose the magnitude of the gain decreases by 3 dB from its dc value at a frequency of 100 kHz when R_2 = 1.0 kΩ. What will be the 3-dB frequency for R_2 = 100 kΩ? Assume the open loop gain decreases at 20 dB per decade.



① First find open loop gain at $f_1 = 100$ kHz with $R_2 = 1\,k\Omega$

For $R_2 = 1\,k\Omega$, the dc gain is $a_{dc} = -R_2/R_1 = -1$

Then at 100 kHz, the gain is 3 dB lower : $a = -1/\sqrt{2}$

so from ★ $\quad 1/\sqrt{2} = \frac{a_o R_2}{R_1 + R_2 + a_o R_1} = \frac{a_o}{2 + a_o}$ $\quad$ (using $R_1 = R_2$).

Solving for a_o, $(2 + a_o) = \sqrt{2}\, a_o \Rightarrow a_o(\sqrt{2} - 1) = 2 \Rightarrow \boxed{a_{o_1} = \frac{2}{\sqrt{2} - 1} = 4.82}$

② Next, find the open loop gain at the 3-dB freq. (f_2) with $R_2 = 100\,k\Omega$

For $R = 100\,k\Omega$, the dc gain is $a_{dc} = -R_2/R_1 = -100 \rightarrow a = -100/\sqrt{2}$ at f_2

so from ★ $\quad 100/\sqrt{2} = \frac{a_o R_2}{R_1 + R_2 + a_o R_1} = \frac{a_o 100}{1 + 100 + a_o}$ $\quad$ (using $R_2 = 100\, R_1$)

Solving for a_o, $a_o + 101 = \sqrt{2}\, a_o \Rightarrow a_o(\sqrt{2} - 1) = 101 \Rightarrow \boxed{a_{o_2} = 244}$

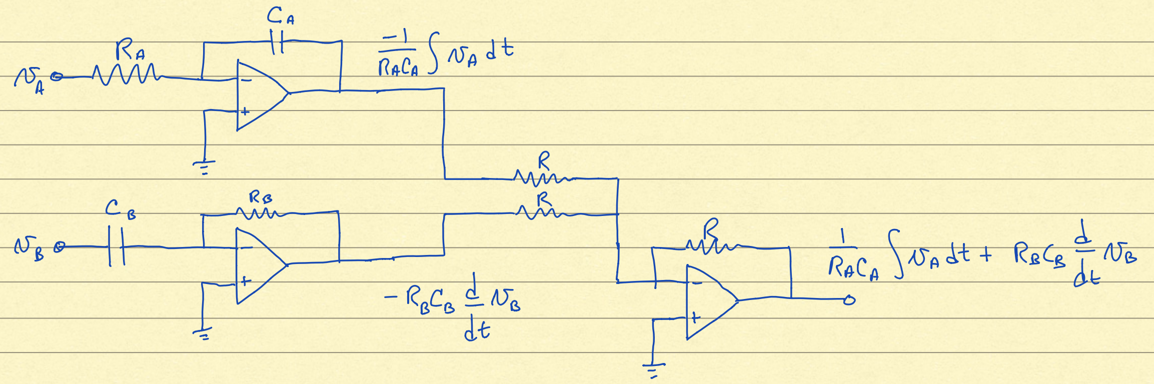
③ Find the 3-dB freq (f_2) in step 2

Since a_o decreases at 20 dB / decade, $\quad 20 \log(a_o) = A - 20 \log(f)$

so $20 \log(a_{o2}) - 20 \log(a_{o1}) = 20 \log f_1 - 20 \log f_2$

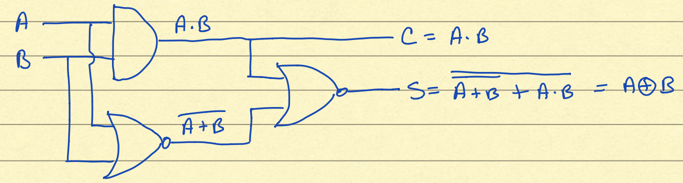
or $\frac{a_{o2}}{a_{o1}} = \frac{f_1}{f_2} \Rightarrow f_2 = f_1 \left(\frac{a_{o1}}{a_{o2}}\right) = 100\,kHz \left(\frac{4.82}{244}\right) \Rightarrow \boxed{f_2 = 1.97\ kHz.}$

(c) Design an op-amp circuit that will take the derivative of one signal and add it to the integral of a second signal. It is not necessary to specify component values.

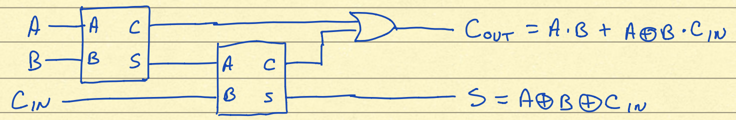


8. (a) A half adder takes two inputs (A, B) and generates two outputs ($A \cdot B$, $A \oplus B$). Using $A \oplus B = \overline{\overline{A+B} + A \cdot B}$, show how to implement a half adder using 3 gates selected from AND, NAND, OR, and NOR. A full adder takes three inputs (A, B, C) and provides two outputs ($A \oplus B \oplus C, A \cdot B + A \oplus B \cdot C$). Show how to implement a full adder using 7 gates.

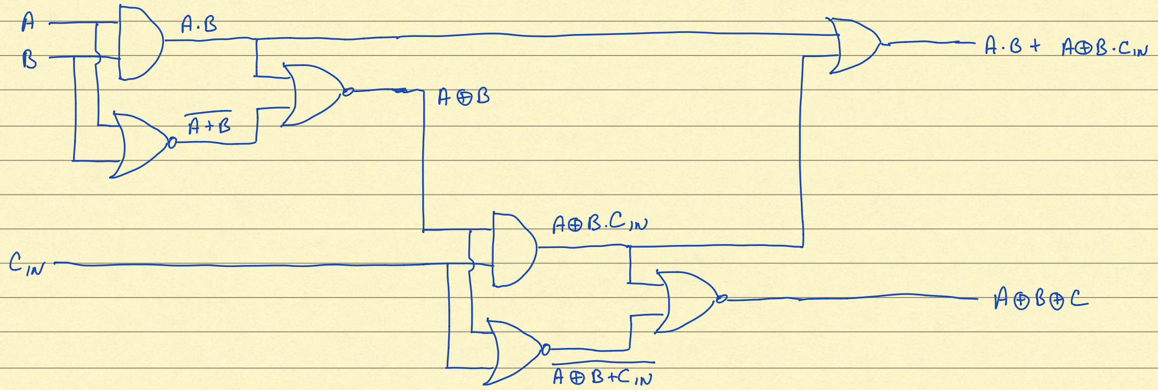
Half adder with 3 gates using $A \oplus B = \overline{\overline{A+B} + A \cdot B}$



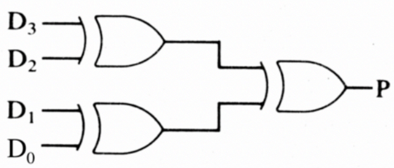
A full adder can be made from 2 half adders and a NOR gate:



Using the 3 gates above for each half adder gives a full adder with 7 gates:

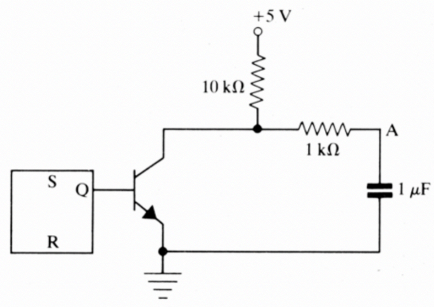


(b) Write the truth table for the following gate schematic. (P is called the parity.)

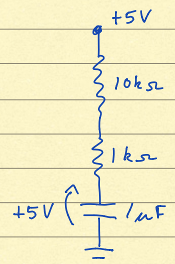


	D_0	D_1	D_2	D_3	$D_0 \oplus D_1$	$D_2 \oplus D_3$	$P = (D_0 \oplus D_1) \oplus (D_2 \oplus D_3)$
0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	1
2	0	0	1	0	0	1	1
3	0	0	1	1	0	0	0
4	0	1	0	0	1	0	1
5	0	1	0	1	1	1	0
6	0	1	1	0	1	1	0
7	0	1	1	1	1	0	1
8	1	0	0	0	1	0	1
9	1	0	0	1	1	1	0
10	1	0	1	0	1	1	0
11	1	0	1	1	1	0	1
12	1	1	0	0	0	0	0
13	1	1	0	1	0	1	1
14	1	1	1	0	0	1	1
15	1	1	1	1	0	0	0

9. (a) Initially $R = S = Q = 0\text{V}$ on the RS flip flop shown below. At time $t = 0$, S goes to 1. Sketch v_A as a function of time.

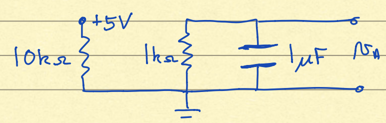


Initially, the transistor is off ($Q=0$), so the circuit can be represented as:



In this configuration, the capacitor will charge to the full 5 V at equilibrium

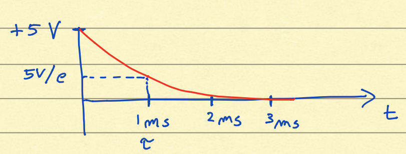
When S (set) goes to logic 1, then $Q \to 1$, and the transistor turns on. Then the circuit can be redrawn as:



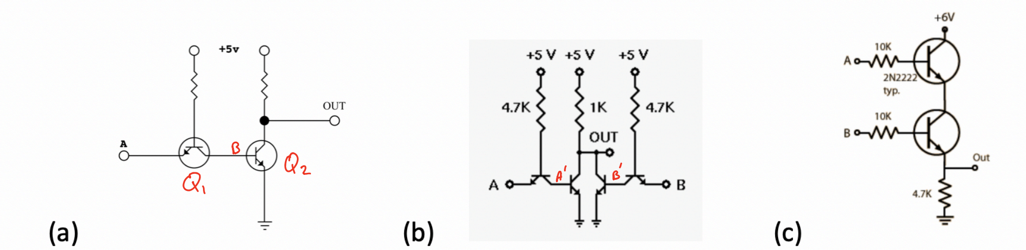
Then the capacitor will discharge from +5V to ground through the 1kΩ resistor:

$v_A = V_0 e^{-t/RC}$. Here $RC = (1\text{k}\Omega)(1\mu\text{F}) = 1\text{ms}$, so

$v_A = +5\text{V}\, e^{-t/(1\text{ms})}$



(b) Identify the function of each of the following gates.



NOT

A	B	OUT
0	0	1
1	1	0

When A is low, Q_1 turn on
B → low
Q_2 → off
OUT → high

When A is high, Q_1 → off
B → high
Q_2 → on
OUT → low

NOR

A	B	OUT	A + B	$\overline{A+B}$
1	1	0	1	0
1	0	0	1	0
0	1	0	1	0
0	0	1	0	1

See part (a) A' follow A
B' follow B

Then if either A or B (or both) are high
the respective transistor(s) → on
and OUT → low

If both A + B are low, both
transistor → off, so
OUT → high

AND

A	B	OUT	A·B
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

If both A and B are high, both transistor are on, so OUT → high

Otherwise one or both are off and
OUT → low