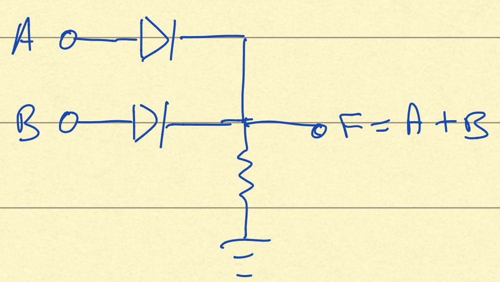
Phys2610 (2019) Assignment 6 solutions

1. Use truth tables to prove that $A \cdot B = B \cdot A$ and $A \oplus B = A \cdot \bar{B} + B \cdot \bar{A}$.

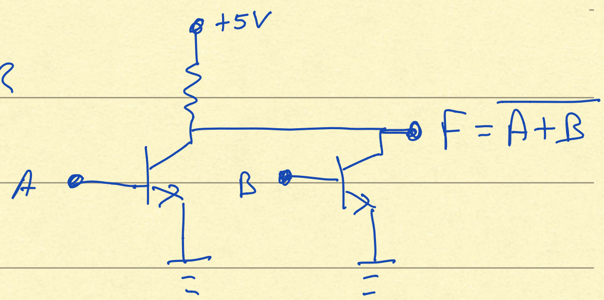
A	B	$A \cdot B$	$= B \cdot A$	$\bar{A}$	$\bar{B}$	$A \cdot \bar{B}$	$B \cdot \bar{A}$	$A \cdot \bar{B} + B \cdot \bar{A}$	$= A \oplus B$
0	0	0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	1	1	1
1	0	0	0	0	1	1	0	1	1
1	1	1	1	0	0	0	0	0	0

2. Using diodes, npn transistors, and resistors, give an example of a circuit diagram for each of the following gates: (a) OR, (b) NOR, (c) AND, (d) NAND, and (e) NOT.

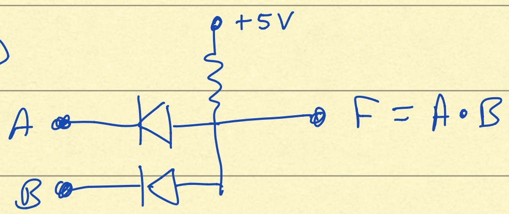
(a) OR



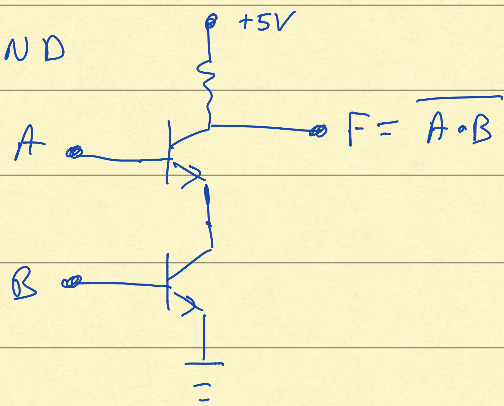
(b) NOR



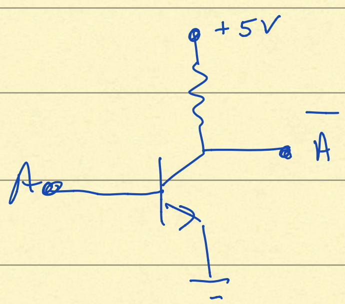
(c) AND



(d) NAND



(e) NOT

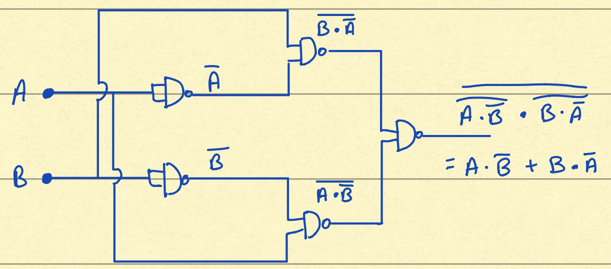


3. Draw a gate schematic to implement exclusive OR using only NAND gates.

$A \oplus B = A\cdot\overline{B} + B\cdot\overline{A}$

$= \overline{\overline{A\cdot\overline{B}}} + \overline{\overline{B\cdot\overline{A}}}$

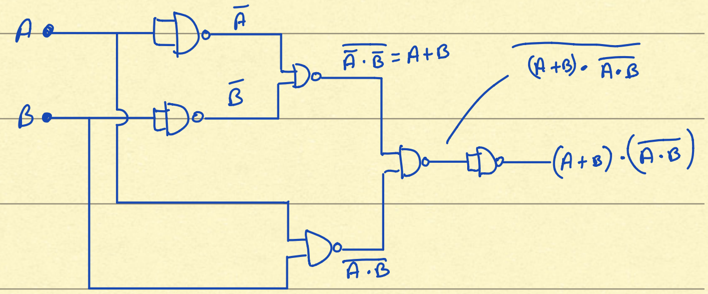
$= \overline{\overline{A\cdot\overline{B}} \cdot \overline{B\cdot\overline{A}}}$ (De Morgan)



or //

$A \oplus B = (A+B)\cdot(\overline{A\cdot B})$

$= \overline{\overline{\overline{\overline{A}\cdot\overline{B}}\cdot\overline{A\cdot B}}}$



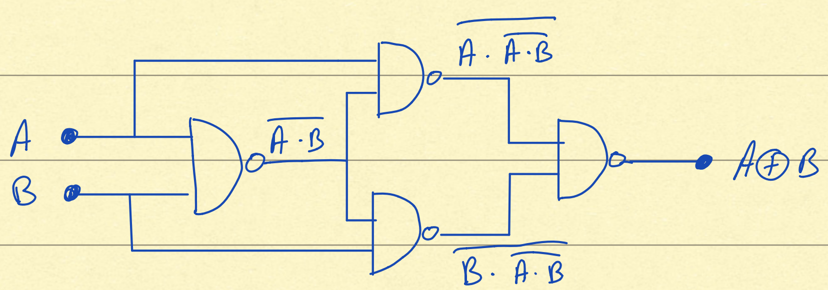
or //

$A \oplus B = (A+B)\cdot\overline{A\cdot B}$

$= A\cdot\overline{A\cdot B} + B\cdot\overline{A\cdot B}$ (distributive)

$= \overline{\overline{A\cdot\overline{A\cdot B}}\cdot\overline{B\cdot\overline{A\cdot B}}}$ (De Morgan)

(most efficient)

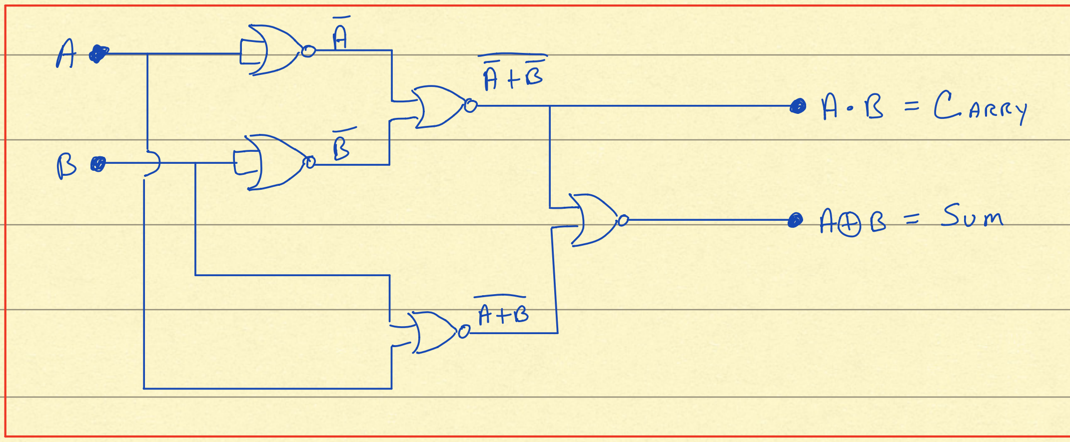


4. Show the explicit diagram for a half adder using only NOR gates. Now show a schematic for a full adder using half adders and NOR gate(s).

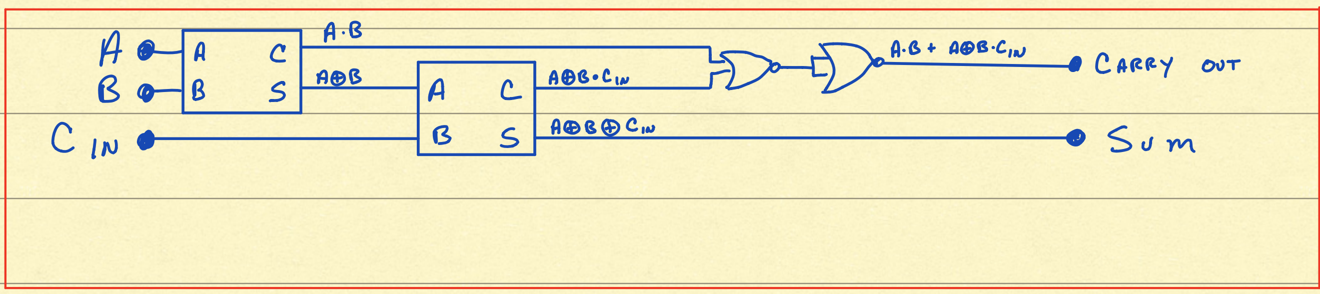
Half adder: $\text{Sum} = A \oplus B = (A+B) \cdot \left(\overline{A \cdot B}\right)$ $\qquad$ $\text{Carry} = A \cdot B = \overline{\bar{A} + \bar{B}}$

$= (A+B) \cdot (\bar{A} + \bar{B})$

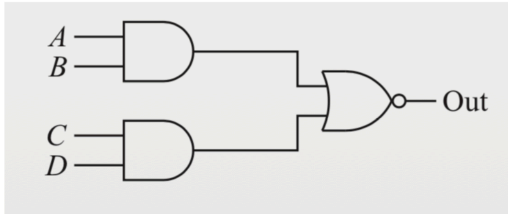
$= \overline{\overline{A+B} + \overline{(\bar{A} + \bar{B})}}$



Full Adder: $\text{Sum} = A \oplus B \oplus C_{IN}$, $\text{Carry} = (A \cdot B) + (A \oplus B) \cdot C_{IN}$

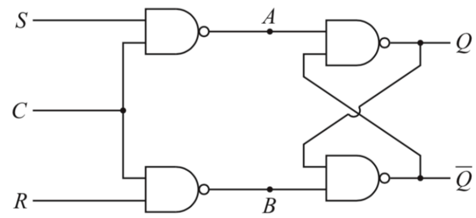


5. Produce the truth table for the AND-OR-INVERT (AOI) gate shown below.



A	B	C	D	$A \cdot B$	$C \cdot D$	$A \cdot B + C \cdot D$	$\overline{A \cdot B + C \cdot D}$
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0

6. Using only NOR gates, produce a clocked flip-flop with the same functionality as the one below (from Section 8.9.2 of the text).

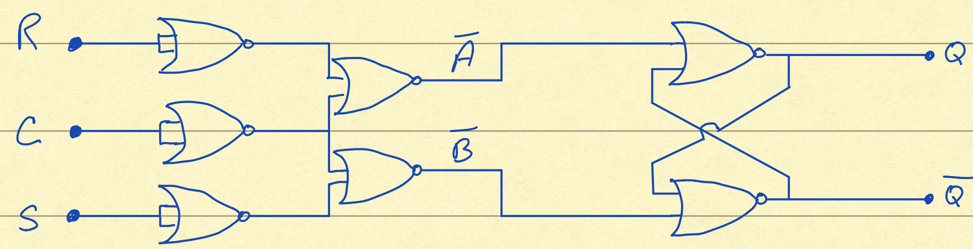


The NAND flip flop behaves like the NOR flip flop with complemented inputs. So, if the NAND flip flop is replaced by a NOR flip flop, we have to generate $\overline{A}$ and $\overline{B}$. But,

$$A = \overline{S \cdot C} \quad \text{and} \quad B = \overline{R \cdot C}$$

$$\text{so} \quad \overline{A} = S \cdot C \quad \text{and} \quad \overline{B} = R \cdot C$$

Using only NOR gates, $\overline{A} = \overline{\overline{S} + \overline{C}}$ and $\overline{B} = \overline{\overline{R} + \overline{C}}$.



Check with truth table:

C	R	S	$\overline{C}$	$\overline{R}$	$\overline{S}$	$\overline{S}+\overline{C}$	$\overline{R}+\overline{C}$	$\overline{A}$	$\overline{B}$	Q (NOR gates)	$\overline{Q}$ (NOR gates)	$\overline{C \cdot S}$ = A	$\overline{C \cdot R}$ = B	Q (NAND gates)	$\overline{Q}$ (NAND gates)
0	0	0	1	1	1	1	1	0	0	NC	NC	1	1	NC	NC
0	0	1	1	1	0	1	1	0	0	↓	↓	1	1	↓	↓
0	1	0	1	0	1	1	1	0	0	↓	↓	1	1	↓	↓
0	1	1	1	0	0	1	1	0	0	↓	↓	1	1	↓	↓
1	0	0	0	1	1	1	1	0	0	↓	↓	1	1	↓	↓
1	0	1	0	1	0	0	1	1	0	1	0	0	1	1	0
1	1	0	0	0	1	1	0	0	1	0	1	1	0	0	1
1	1	1	0	0	0	0	0	1	1	X	X	0	0	X	X